340375 - ESC2-I3O01 - Computer Structure II

Coordinating unit: 340 - EPSEVG - Vilanova i la Geltrú School of Engineering
Teaching unit: 701 - AC - Department of Computer Architecture
Academic year: 2017
Degree: BACHELOR'S DEGREE IN INFORMATICS ENGINEERING (Syllabus 2010). (Teaching unit Compulsory)
ECTS credits: 6
Teaching languages: Catalan, Spanish

Teaching staff
Coordinator: Eva Marín Tordera

Degree competences to which the subject contributes

Specific:
1. CEFC1. Ability to design, develop, select and value applications and informatic systems affirming its reliability, security and quality corresponding to ethical principals and legislation and current rules.
2. CEFC13. Knowledge and application of necessary tools for storage, processing and access to informatic systems, including the ones based on webs.
3. CEFC4. Ability to work out technical conditions of an informatic installation observing standard and current rules.
4. CEFC7. Knowledge, design and efficient use of data types and structures the most appropriate to resolve problems.
5. CEFC9. Ability to know, understand and assess computer structure and architecture, as well as basic components forming them.

Transversal:
7. SUSTAINABILITY AND SOCIAL COMMITMENT - Level 2. Applying sustainability criteria and professional codes of conduct in the design and assessment of technological solutions.
6. THIRD LANGUAGE. Learning a third language, preferably English, to a degree of oral and written fluency that fits in with the future needs of the graduates of each course.

Learning objectives of the subject

Deeper knowledge of the structure of computers, as well as in the design and implementation of small micro-computer based systems. Specifically, it aims to understand and delve into the internal structures and the memory hierarchy (disk, main memory, caches, mechanisms for error detection and correction) in the concepts of concurrency, input / output and buses (survey, interruptions, DMA, types of I / S), and firmware programming of a microcomputer will also be addressed.
### Study load

<table>
<thead>
<tr>
<th>Total learning time: 150h</th>
<th>Hours large group: 45h</th>
<th>30.00%</th>
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<tbody>
<tr>
<td></td>
<td>Hours medium group: 0h</td>
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<tr>
<td></td>
<td>Hours small group: 15h</td>
<td>10.00%</td>
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<tr>
<td></td>
<td>Guided activities: 0h</td>
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<tr>
<td></td>
<td>Self study: 90h</td>
<td>60.00%</td>
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# Content

<table>
<thead>
<tr>
<th>1. Input/output</th>
<th>Learning time: 39h</th>
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<tbody>
<tr>
<td><strong>Description:</strong></td>
<td>Theory classes: 4h</td>
</tr>
<tr>
<td>1. Devices E/S: Polling</td>
<td>Practical classes: 8h</td>
</tr>
<tr>
<td>1.2. Synchronizing E/S for Interruptions</td>
<td>Laboratory classes: 4h</td>
</tr>
<tr>
<td>1.2.B Exceptions</td>
<td>Guided activities: 2h</td>
</tr>
<tr>
<td>1.3. Direct Memory Access (DMA)</td>
<td>Self study : 21h</td>
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**Related activities:**
- Activity 1: Problems Input / Output
- Activity 2: Lab 1 of synchronization by polling
- Activity 2: Lab 2 of synchronization by interruptions
- Activity 4: Partial test of knowledge

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<thead>
<tr>
<th>2. Cache Memory</th>
<th>Learning time: 30h</th>
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<tbody>
<tr>
<td><strong>Description:</strong></td>
<td>Theory classes: 4h</td>
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<tr>
<td>2.1. Introduction to Memory Hierarchy</td>
<td>Practical classes: 7h</td>
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<tr>
<td>2.2. Cache memory</td>
<td>Laboratory classes: 2h</td>
</tr>
<tr>
<td>2.3. Impact of the Organization of memory cache performance</td>
<td>Guided activities: 2h</td>
</tr>
<tr>
<td>2.4. Performance Measures</td>
<td>Self study : 15h</td>
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<tr>
<td>2.5 Design Considerations and cache controller</td>
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**Related activities:**
- Activity 1: Cache memory exercises
- Activity 2: Memory cache lab
### (ENG) 3. Memoria Virtual

**Learning time:** 20h  
Theory classes: 2h  
Practical classes: 4h  
Laboratory classes: 2h  
Guided activities: 2h  
Self study: 10h  

**Description:**  
3.1. Introduction  
3.2. Address translation and pagination  
3.3. Integrating virtual memory and cache  

**Related activities:**  
Activity 1: Virtual memory exercises

### 4. Microprogramming

**Learning time:** 29h  
Theory classes: 3h  
Practical classes: 6h  
Laboratory classes: 2h  
Self study: 18h  

**Description:**  
4.1. Revision Control Unit (INCO)  
4.2. Types of Control Unit  
4.3. Microprogrammed control unit  

**Related activities:**  
Activity 1: Microprogramming exercises  
Activity 3: Work directed  
Activity 4: Test of knowledge

### Qualification system

Final Mark = (Partial examination) * 0.25 + (Exercises) * 0.1 + (Lab) * 0.2 + (Complementary work) * 0.1 + (Final examination) * 0.35 >= 5

### Bibliography

**Basic:**  